International Journal on Emerging Technologies **8**(2): 13-18(2017)

ISSN No. (Print) : 0975-8364
ISSN No. (Online) : 2249-3255

New Low Power 1-bit Full Adder Circuit for Speed in Nanoscale Technology

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(Received 02 October, 2017 accepted 10 November, 2017)
(Published by Research Trend, Website: www.researchtrend.net)

ABSTRACT: Adders are one of the most basic building blocks in digital components present in the Arithmetic Logic Unit (ALU). The performance of an adder have a significant impact on the overall performance of a digital system. In this paper we presented a new 13T full adder design based on hybrid – CMOS logic design style. The new design is compared with some existing designs for power consumption, delay, PDP at various frequencies. It is found that the existing Static Energy Recovery Full (SERF) adder and Gate Diffusion Input (GDI) full adder provides poor performance when compared with proposed adder cell and also its equivalent layout has been generated to calculate the area of existing and proposed adder cell by using Microwind 3.5 tool. From the simulation result it is observed that the first proposed adder circuit using XOR module has achieved maximum saving of PDP 46.71% & 96.61% when compared to existing SERF and GDI adder cells respectively. The second proposed circuit using XNOR module has achieved maximum saving of PDP 74.59% & 98.38% when compared to existing SERF and GDI 1-bit adder cells respectively.

Keywords: Full adder, Conventional adder, GDI, SERF, CMOS Adder.

I. INTRODUCTION

Efficiency of implementation of arithmetic circuits in the execution of dedicated algorithms such as digital filtering, correlation and convolution largely affects the performance of application specific integrated circuits and digital signal processors. The increasing density of transistors hence complexity in the integrated circuits demands for high speed, power efficient designs. The researchers over the time have developed numerous CMOS Logic styles to meet the requirement of the rapidly growing industry. Lowering the supply voltage is a means of reducing the power consumption of the circuit in ultra deep submicron technology but it results in degraded driving capability and increased circuit delay of the designed cells.

Full adder proves to be the most fundamental circuit employed in many complex arithmetic operations such as addition, subtraction, division, multiplication, exponentiation etc [1-2]. Adder circuit must have a fast carry generation mechanism because the critical path in the above mentioned applications generally goes along the entire carry-in to carry-out path of the full adders. Slower carry-out generation results as increase in worst case delay and glitches in the later stages, which leads to higher power consumption. The full adder circuit also demands for simultaneous generation of the sum and carry output to reduce glitches in the lower stages of the full adder.

The rapid increase in demand of portable battery operated devices has urged for low power and high speed devices and various logic styles have been developed over the years to fulfill these goals. The most basic design is the conventional static CMOS full adder [3,4] which comprises of a regular CMOS structure. The adder provides full voltage swing output with good driving capability owing to the conventional pull up and pull down transistors structure. The large number of PMOS transistors used in the design result in high input capacitance, declined speed and more area. Complementary transistor logic (CPL) is another conventional design which provides full voltage swing and good driving capability at high speed with increased number of internal nodes and transistors, Although this increases the power dissipation in the circuit [5]. Another modern design technique is the GDI (gate diffusion input) technique. the adders based on GDI technique utilize a regular GDI cell structure to carry out adder functionality.

The primary disadvantage of the GDI adder is degraded voltage swing at the output which results in reduced driving capability [6,7]. The floating adder circuit is another high speed low power design which good low power characteristics and robust performance at frequencies of the order of 1GHz. The only disadvantage of floating adder is the respective weak '0' and '1' logic produced at its sum and carry output. The endeavors of the researchers have led to continuous reduction in chip area and power dissipation in the circuit, the 8 transistor adder described in [8] is one of such circuits. The adder occupies very small area due to small number of transistors but the circuit has large degradation in the output voltage swing due to the threshold losses hence it has very poor driving capability. The SERF adder described in [9] is also a low power design of the full adder but the circuit fails to operate well at lower supply voltages.

Recently, the GDI (Gate Diffusion Input) technique is emerged as a promising alternative to Standard CMOS Logic [4]. The GDI technique has reduced power dissipation and less delay with least number of transistor counts in design of any digital system. Similar to other existing techniques, GDI also suffers from low output swing voltage problem due to low threshold voltage [5]. This research work tried to overwhelm this problem by adding an additional pass transistor to GDI cell. Implementations of proposed method in few digital circuits provide better result in terms of power reduction and delay.

The rest of paper is organized as- In section 1 we have discussed about introductory part of 1-bit full adder, various type of existing adder is discussed in section 2, proposed work is discussed in section 3, later simulation and results are discussed in section 4 and conclusion is discussed in section 5.

II. LITRATURE SURVEY

The conventional CMOS full adder comprises of a regular CMOS structure of 28 transistors with usual pull-up and pull-down networks as shown in Fig.1 [7]. The complementary design of CMOS full adder accounts for full output voltage swing and its robustness against voltage scaling and transistor sizing is one of its main advantages. The main drawback of C-CMOS adder is its large input capacitance due to the utilization of large number of PMOS transistors in its design. The large number of PMOS transistors also increases the chip area required for the circuit.

One bit full adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. Two inputs (A, B) are the bits to be added, the third input (C_{in}) represents the carry form the previous position. Two outputs are sum (S) and output carry (C_{out}). Truth table for full-adder is shown in Table 1.

Table 1: Truth Table of Full-Adder.

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The Karnaugh map method [21] is used to find the algebraic expressions for the two output variables of full adder. Simplified expression for the output variables sum (S) and output carry (C_{out}) are given in following s [3]:

$$S = (A \oplus B) \oplus C_{in} \quad (1)$$

$$C_{out} = (A \oplus B) C_{in} + (\overline{A \oplus B})\, A \quad (2)$$

From the above s, the logic diagram for full adder can easily draw in Fig. 1.

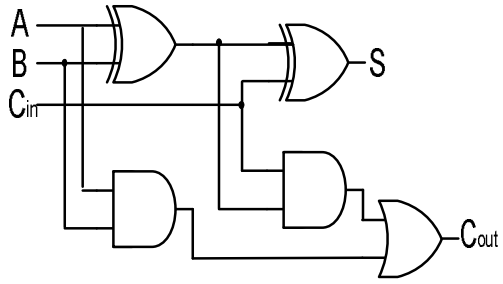

Fig. 1. Gate level logic diagram of full adder.

The full adder is implemented by two XOR gates, two AND gates and OR gate. The given XOR gates are used to obtain the sum output of the full-adder and other logic gates are used to get the carry output of the full-adder.

A. C-CMOS Full Adder Cell

The conventional C-CMOS 1-bit adder cell using 28 transistors is based on standard CMOS topology as shown in Fig. 2. Due to large number of transistors used in designing it's power consumption is high and the critical path with the input of the circuit consist of 5 transistors in its forward path so propagation delay is more [1-4, 6, 13]. This design does not uses compliment of input signals and therefore the short circuit current is reduced and the most important advantage of this circuit is it produces full output voltage swing, thus this circuit has high noise margin that is why it is reliable to operate at the low voltages.

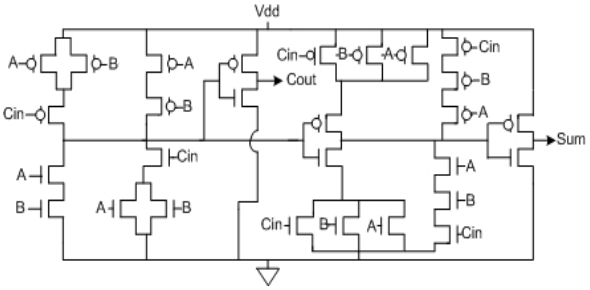

Fig. 2. C-CMOS Full Adder Cell (Conventional full adder cell).

B. Static Energy Recovery Full Adder Cell

Static Energy Recovery Full (SERF) adder requires ten transistors (10T) to implement it [7-10,13]. It can be implemented by using XOR or XNOR gates, Fig. 3 shows implementation of SERF with the help of XOR gates. To produce sum output it uses two cascaded XOR gates. Here is threshold loss problem in SERF circuit and the result of these output signals (Sum, Cout) will not provide full swing of voltages means degradation of output signal take place which is not at all desirable condition for cascaded structure. Main disadvantage of SERF along with output logic swing is that both the power dissipation and delay are more. The advantage of SERF is that it uses the least number of transistors in designing so the chip area is reduced and also it should be noted that the SERF adder cell has no direct path with the ground. Because of non existence of ground path it reduces power consumption.

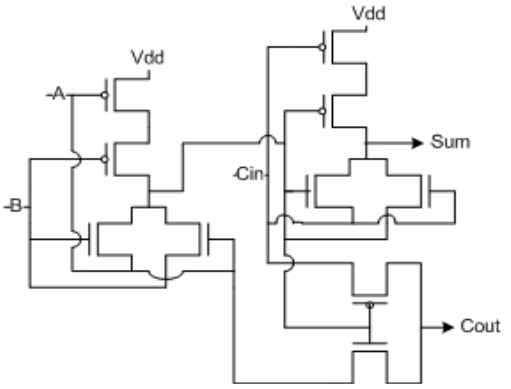

Fig. 3. SERF Adder Cell (10T).

C. Gate Diffusion Input Full Adder Cell

The design of Gate Diffusion Input (GDI) full adder cell consists of two XOR/XNOR gates, GDI circuit implemented in this paper consist of two XOR gates which are designed by using four transistors each as shown in Fig.4 [11, 12]. The GDI full adder cell requires 10 transistors, which is very less in number as compared to conventional CMOS design and the speed is also more as compared conventional CMOS design. But in other hand GDI technique suffers from voltage swing degradation due to voltage loss problem and also the major problem of a GDI full adder cell is that it requires twin-well CMOS or Silicon On Insulator (SOI) process to construct it, so it will be more expensive to implement a GDI chip. If GDI uses only standard p-well CMOS process to implement it, the new problem arises that is decrease in driving capability which makes this process more expensive and also not easy to realize.

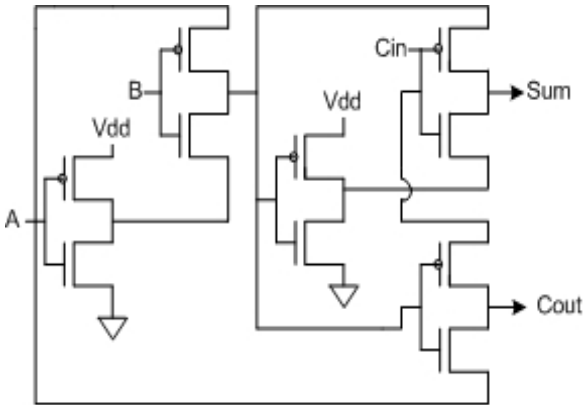

Fig. 4. GDI full Adder Cell (10T)

III. PROPOSED WORK

The hybrid logic design style involves the division of larger circuit into smaller sub-circuits and each sub-circuit is optimized using various logic design style. The hybrid design methodology for a full adder circuit is shown in Fig.5. As shown in the figure the full adder circuit is divided into three modules and these modules are designed using various different design styles to exploit the advantages of the different design styles and extract the desired performance. Module 1 produces XNOR and XOR functions of the inputs A and B [15,16]. The module1 can be either XNOR based or XOR based depending on the primary output generated within the module the primary output is utilized to get the other output using an inverter. Module 2 and Module 3 comprises of the circuitry to produce the desired sum and carry outputs of the full adder by utilizing the intermediate outputs generated by Module 1 circuit.

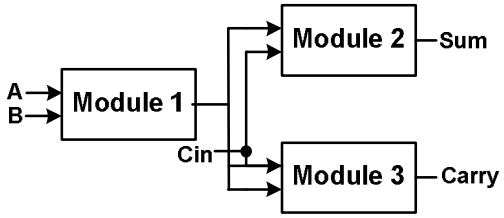

Fig. 5. Hybrid design methodology.

In this paper a 13 transistor design of a single bit full adder based on Hybrid GDI logic design style is been proposed as shown in Fig.6. As the design suggests the proposed adder circuit exploits the advantages of GDI technique, pass transistor technique and transmission gate technique to carryout excellent low power and high speed characteristics.

These two proposed circuits are giving better power and delay as compared with the existing 10T structure i.e. SERF and GDI. The problem with SERF and GDI one bit full adder is output voltage swing which is also present in proposed 1-bit adder cell but it has better performance (less delay), lesser power consumption and efficiently less power delay product.

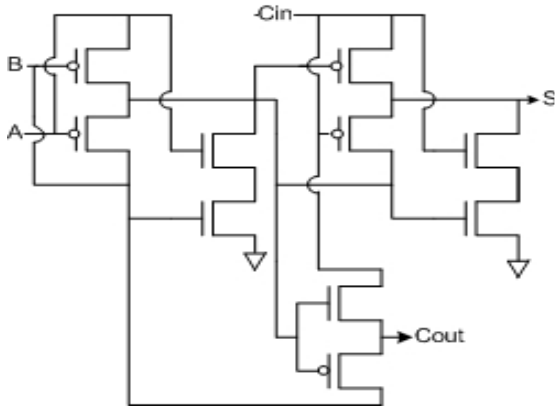

Fig. 6. Proposed full adder cell using XOR module.

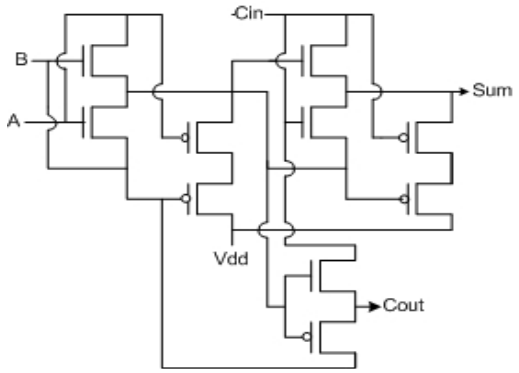

Fig. 7. Proposed full adder cell using XNOR module.

IV. RESULT AND SIMULATION

The simulation part which is performed of existing and proposed adder circuit at the same parameters as shown in Table 2, it shows the calculation of power, delay and power delay product of the proposed adder along with the existing adders at room temperature (25°c) with applied Vdd=1V and operating frequency 100MHz. These results are calculated by using Synopsys HSPICE tool at 32nm MOSFET technology and it is clearly seen that the power consumption, delay and PDP of the both proposed circuit is better than the existing SERF and GDI at the same numbers of transistors count.

From the tabular comparison presented below it can easily be seen that the proposed circuit show improvements in both power consumption and propagation delay of the circuits and hence an improved power delay product (figure of merit in a digital circuit) is observed.

Table 2: Average power, Delay and PDP at Vdd = 1V.

Parameters	Transistor Count	Avg. Power (E-9W)	Delay (E-11S)	PDP (E-20J)
C-CMOS (28T)	28	10.634	7.9783	84.841
SERF (10T)	10	11.813	1.8350	21.676
GDI (10T)	10	59.737	5.6984	340.40
Proposed-1 (10T)	10	4.9899	2.3152	11.551
Proposed-2 (10T)	10	4.1577	1.3245	5.5068

Table 3 shows the variation in power of proposed and existing adders at different temperature, as the temperature increase the power consumption also increase. The variation in power consumption of GDI at different temperature is more as compared to proposed adder circuits.

Table 3: Temperature Vs Average Power at Vdd=1V.

Parameters	Power at respective Temperature (nW)				
	20°C	40°C	60°C	80°C	100°C
C-CMOS (28T)	10.496	10.628	10.910	11.476	11.703
SERF (10T)	11.733	12.015	12.276	12.748	12.973
GDI (10T)	58.741	62.888	68.226	73.830	75.602
Proposed-1 (10T)	4.9590	5.0819	5.3871	5.4530	5.5789
Proposed-2 (10T)	4.0580	4.4555	5.1422	5.5081	5.5785

The proposed circuit consumes desired power till the frequency 1GHz beyond this frequency power consumption increases rapidly as shown in table 4. The proposed circuit using the XNOR can be used till the operating frequency 10GHz this has very less power consumption as compare to all full adder cell.

At 1v operating voltage (Vdd) Conventional adder cell gives proper output voltage swing i.e. 1v at the both output (Sum, Cout) terminals of the adder cell that means in conventional adder cell no degradation of output voltage take place. But at Vdd 1v in SERF adder cell 0.615v output voltage swing take place and for GDI adder cell 0.65v output voltage swing take place, this output voltage degradation problem occur in both SERF and GDI adder cell which is not a desirable condition to operate these adder cell at low input voltage.

Table 4: Frequency Vs Power at Vdd=1V.

Parameters	Power at respective Frequency (nW)			
	10MHz	**100MHZ**	**1GHz**	**10GHz**
C-CMOS (28T)	1.2259	10.634	96.172	7124.4
SERF (10T)	1.2462	11.813	117.92	1983.4
GDI (10T)	44.215	59.737	283.84	2589.6
Proposed-1 (10T)	0.6230	4.9899	50.992	1969.2
Proposed-2(10T)	0.3019	4.1577	45.260	881.51

In proposed adder cell by using XOR module at 1v Vdd 0.6v output voltage swing take place for the carry output (Cout), and in second proposed adder cell i.e. in XNOR module output voltage swing is 0.62v arise for carry output. The problem of degraded output voltage is also remain in the proposed adder cells which is clearly seen in transient analysis of proposed adder cell as shown in Fig.8 and Fig.9.

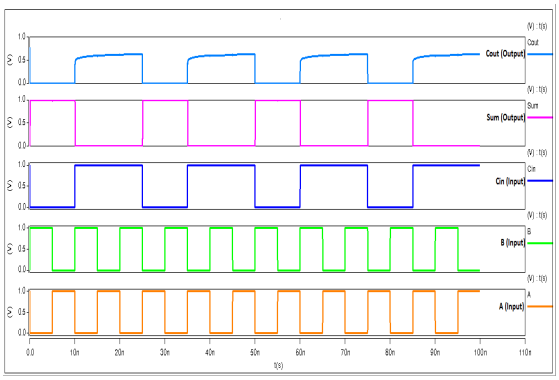

Fig. 8. Transient analysis of proposed one bit full adder cell using XOR module.

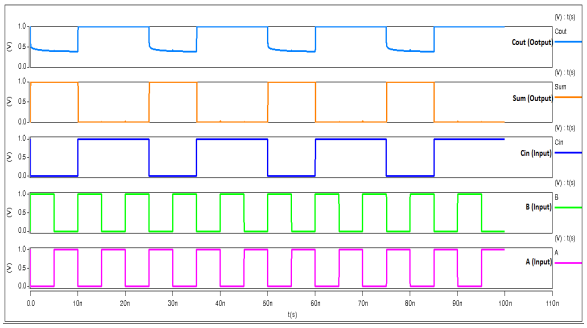

Fig. 9. Transient analysis of proposed one bit full adder cell using XNOR module.

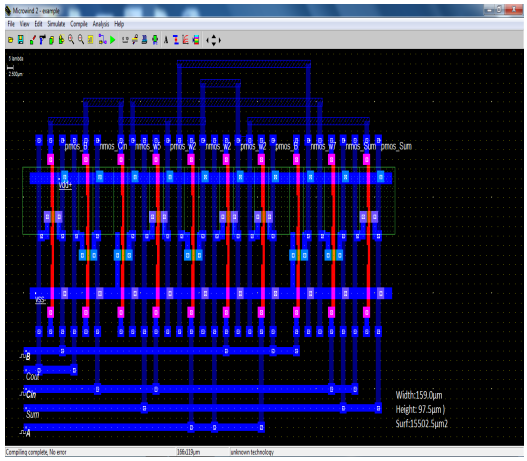

Fig. 10. Layout of proposed full adder cell using XOR module.

Fig. 8 & Fig.9 shows the transient response of proposed full adder cell using XOR and XNOR modules simultaneously at 32nm CMOS technology. The layouts of proposed circuit have been generated by using Microwind 3.5 tool at 32nm CMOS technology and also height, width and surface area of proposed circuits has been calculated. Fig.10 & Fig.11 shows the layouts of corresponding proposed modules.

IV. CONCLUSION

In this paper, two new full adder circuits have been proposed and corresponding simulation results have been generated and then compared with existing adder circuits at 32nm CMOS technology using HSPICE tool. According to the simulation results it is observed that the proposed designs have achieved maximum saving of power 64.80% and 93.04%, maximum reduction in delay 27.82% and 76.75% and maximum saving of PDP 74.59% and 98.38% when compared to the existing SERF and GDI adder respectively.

The proposed circuits are also giving better performance at different temperatures and also at different operating frequencies as compare to existing adder circuits. The proposed circuit is well performing below the operating frequency 1GHz, as we go beyond this frequency its power consumption increases rapidly and also multiple threshold problem arises at output logic levels but still proposed circuit (using XNOR module) consumes less power compared to all existing adder circuit till 10 GHz operating frequency.

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